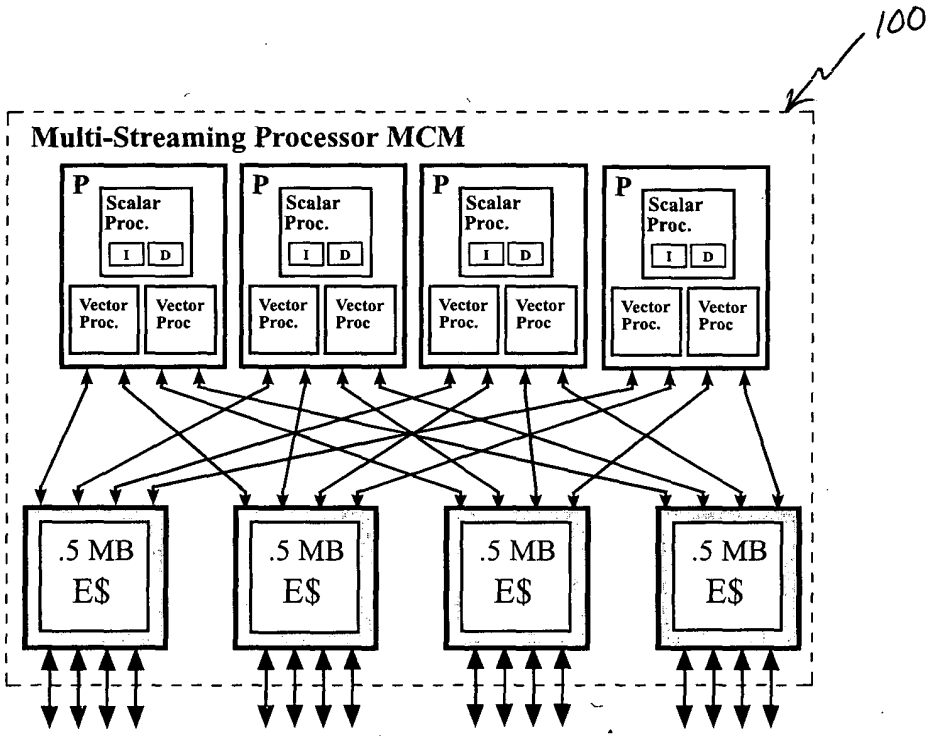
100
Multi-Streaming Processor MCM
P
Scalar Proc.
I
D
Vector Proc.
Vector Proc
.5 MB E$

FIG. 1A

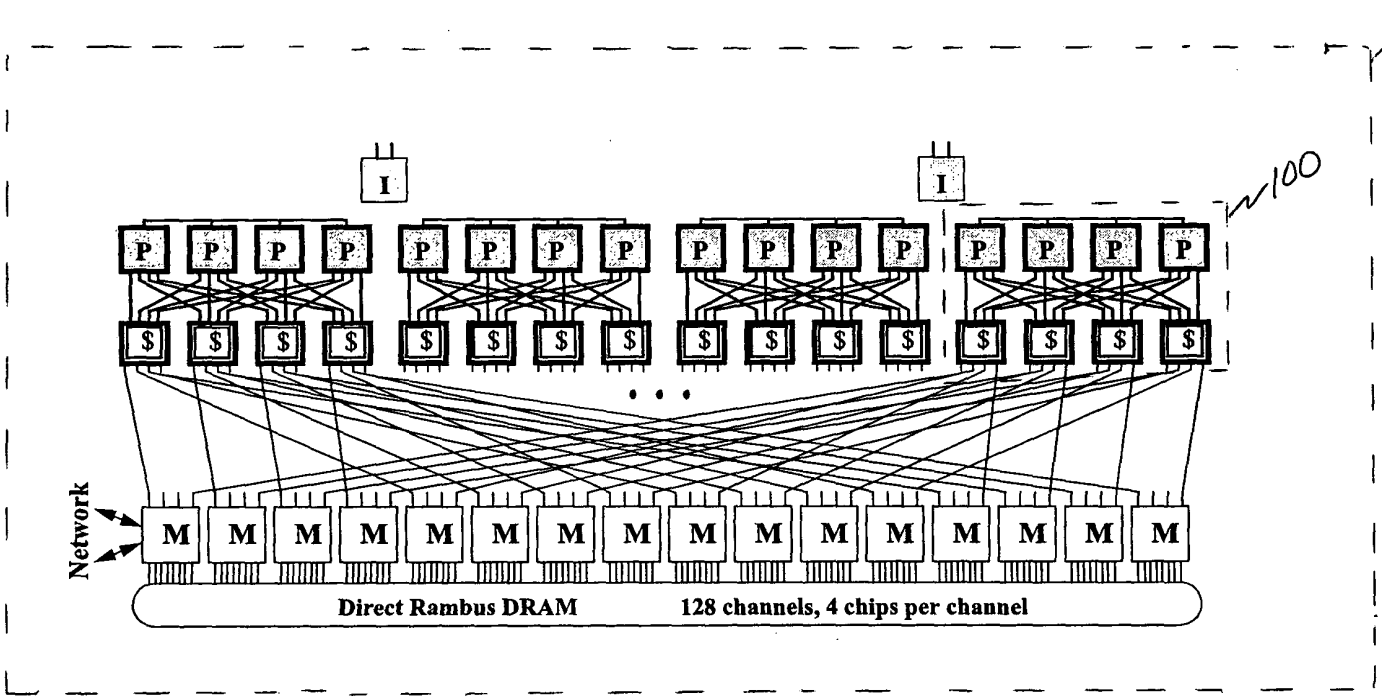
102
100
I
I
P
$
M
Network
Direct Rambus DRAM
128 channels, 4 chips per channel

FIG. 1B

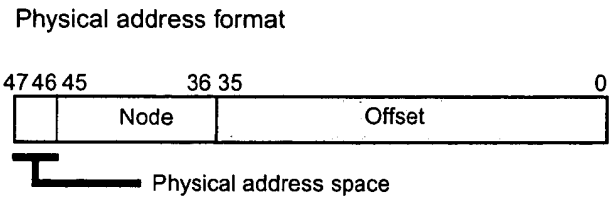
Physical address format
47 46 45
36 35
0
Node
Offset
Physical address space

FIG. 2A

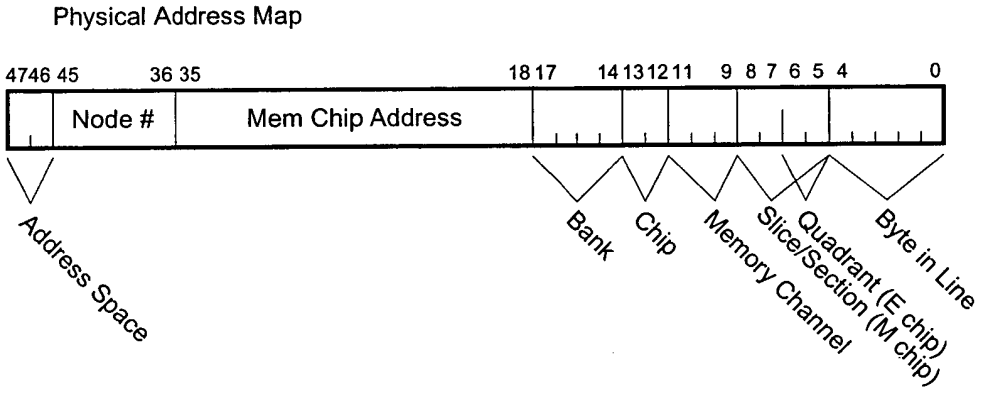
Physical Address Map
47 46 45
36 35
18 17
14 13 12 11
9 8 7 6 5 4
0
Node #
Mem Chip Address
Address Space
Bank
Chip
Memory Channel
Slice/Section (M chip)
Quadrant (E chip)
Byte in Line

FIG. 2B

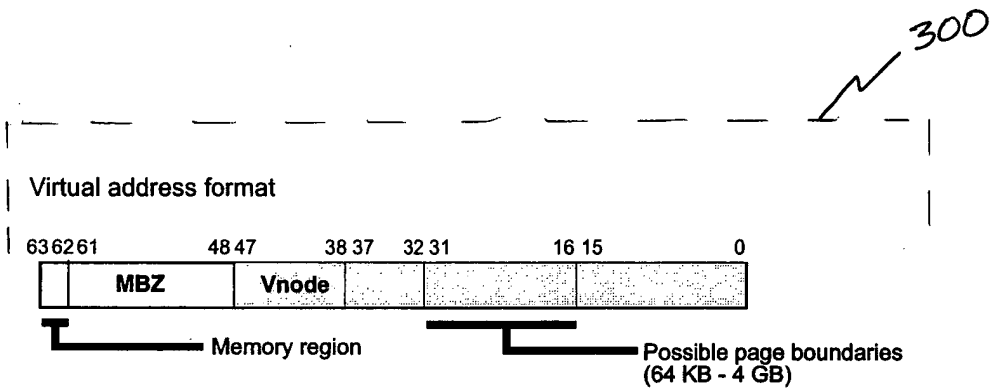
300
Virtual address format
63 62 61
48 47
38 37
32 31
16 15
0
MBZ
Vnode
Memory region
Possible page boundaries
(64 KB - 4 GB)

FIG. 3

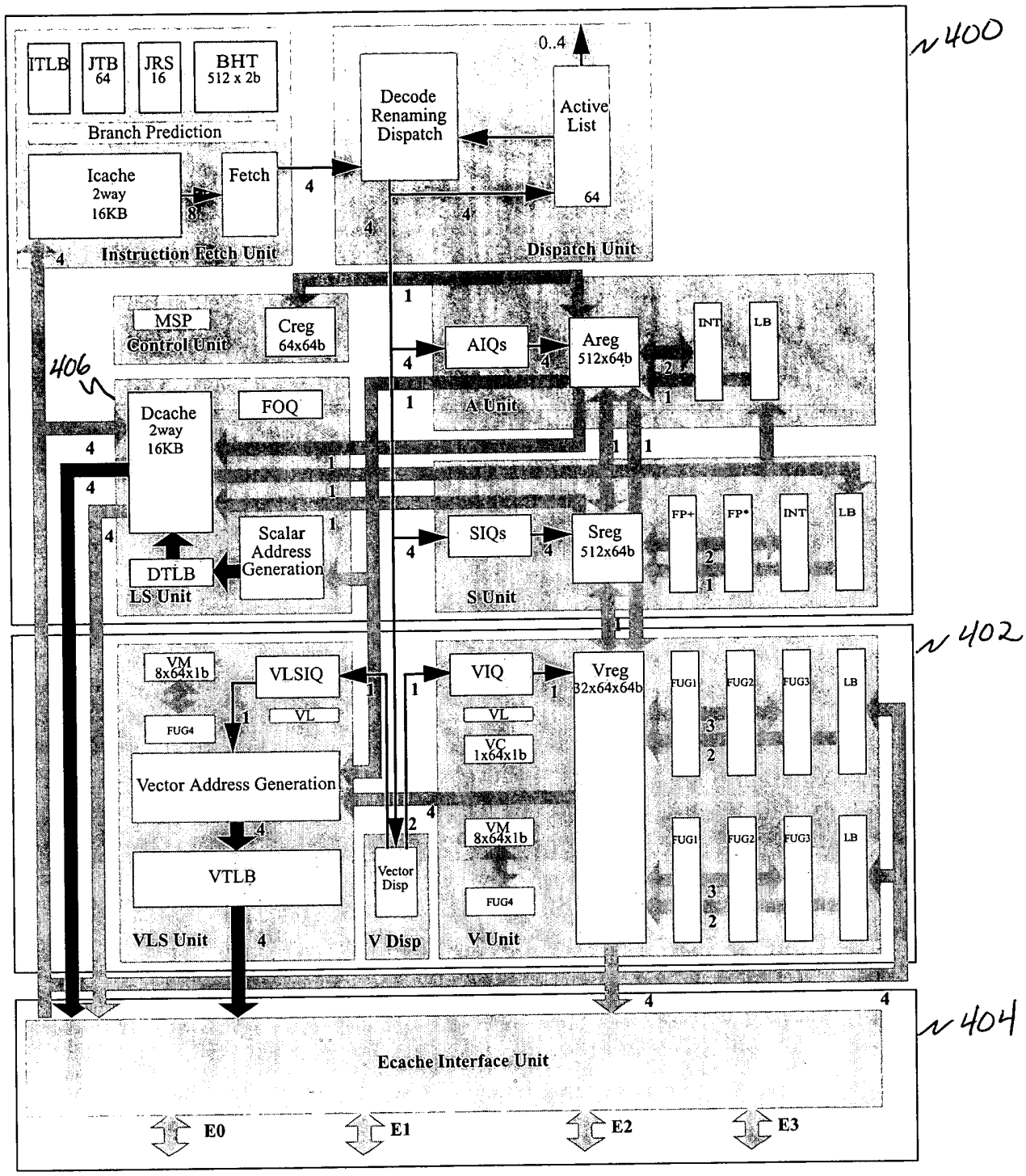
400
ITLB
JTB 64
JRS 16
BHT 512 x 2b
Branch Prediction
Icache 2way 16KB
Fetch
Instruction Fetch Unit
Decode Renaming Dispatch
Active List
0..4
64
Dispatch Unit
MSP Control Unit
Creg 64x64b
AIQs
Areg 512x64b
INT
LB
A Unit
406
Dcache 2way 16KB
FOQ
Scalar Address Generation
DTLB
LS Unit
SIQs
Sreg 512x64b
FP+
FP*
INT
LB
S Unit
402
VM 8x64x1b
VLSIQ
VL
FUG4
Vector Address Generation
VTLB
VLS Unit
Vector Disp
V Disp
VIQ
VL
VC 1x64x1b
VM 8x64x1b
FUG4
V Unit
Vreg 32x64x64b
FUG1
FUG2
FUG3
LB
404
Ecache Interface Unit
E0
E1
E2
E3

FIG. 4A

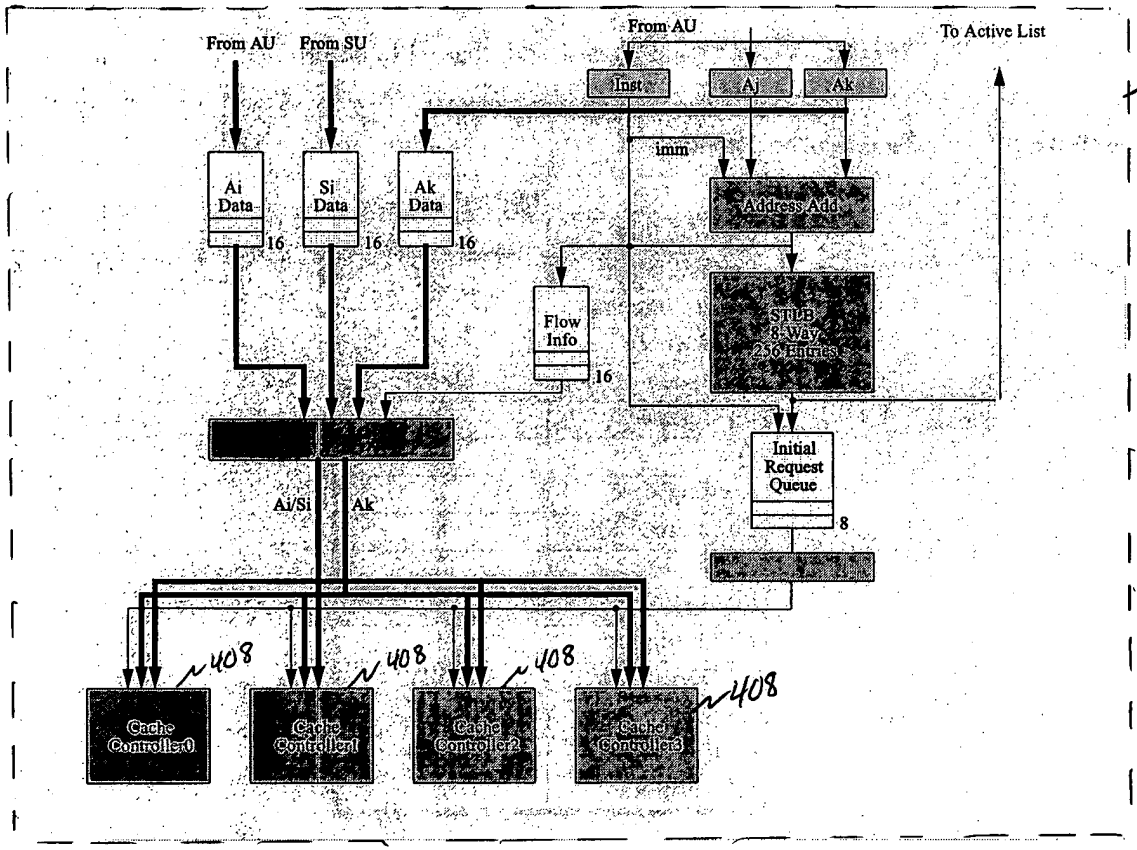
From AU
From SU
From AU
To Active List
406
Inst
Aj
Ak
imm
Ai Data
Si Data
Ak Data
16
16
16
Address Add
Flow Info
16
STLB 3-Way 256 Entries
Initial Request Queue
8
Ai/Si
Ak
408
408
408
408
Cache Controller0
Cache Controller1
Cache Controller2
Cache Controller3

FIG. 4B

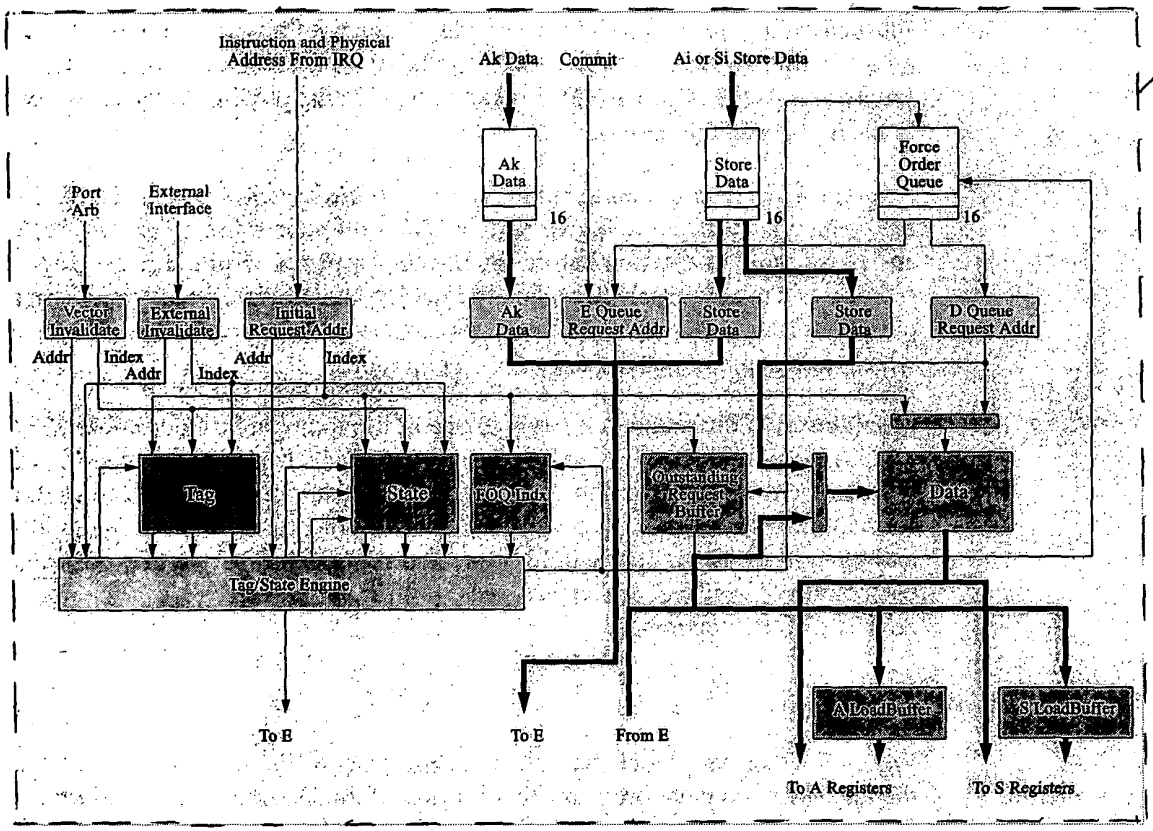
Instruction and Physical Address From IRQ
Ak Data
Commit
Ai or Si Store Data
408
Ak Data
Store Data
Force Order Queue
16
16
16
Port Arb
External Interface
Vector Invalidate
External Invalidate
Initial Request Addr
Ak Data
E Queue Request Addr
Store Data
Store Data
D Queue Request Addr
Addr
Index
Addr
Index
Addr
Index
Tag
State
FOQ Indx
Outstanding Request Buffer
Data
Tag/State Engine
To E
To E
From E
A LoadBuffer
S LoadBuffer
To A Registers
To S Registers

FIG. 4C

Dcache Bypass	Initial Request	Tag & State	FOQ Index Match	Action								
				Msg to E	D$	FOQ entry	E	D	P	Allocate	ORB Entry	Other
No	Read	Miss	No	Read		Dummy		x	x	LRU Way	Read	
			Yes			ReadUC	x				Read nc†	
		Hit	No		Read							
			Yes‡			Read		x				
	ReadShared	Miss	No	ReadShared		Dummy		x	x	LRU Way	Read	
			Yes			ReadUC-Shared	x				Read nc	
		Hit	No		Read							
			Yes††			Read		x				
	ReadNA	Miss	No	ReadNA							Read nc	
			Yes			ReadNA	x				Read nc	
		Hit	No		Read							
			Yes			Read		x				
	Write	Miss	No	ReadMod		SWrite	x	x	x	LRU Way	Read	
			Yes			SWrite	x					
		Hit	No			SWrite	x	x				
			Yes									
	WriteNA	Miss	No			SWriteNA	x					
			Yes									
		Hit	No			SWrite	x	x				
			Yes									
	Prefetch (to discard)	Miss	No									Discard
			Yes									
		Hit	No									
			Yes									

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FIG. 4D

Dcache Bypass	Initial Request	Tag & State	FOQ Index Match	Action								
				Msg to E	D$	FOQ entry	E	D	P	Allocate	ORB Entry	Other
Yes	Read	Miss	No			ReadUC	x				Read nc	
			Yes									
		Hit	No							Invalidate		
			Yes									
	ReadShared	Miss	No			ReadUC-Shared	x				Read nc	
			Yes									
		Hit	No							Invalidate		
			Yes									
	ReadNA	Miss	No			ReadNA	x				Read nc	
			Yes									
		Hit	No							Invalidate		
			Yes									
	Write	Miss	No			SWrite	x					
			Yes									
		Hit	No					x				
			Yes									
	WriteNA	Miss	No			SWriteNA	x					
			Yes									
		Hit	No					x				
			Yes									
	Prefetch (to discard)	Miss	No									Discard
			Yes									
		Hit	No									
			Yes									
	IORead					ReadNA to IO space	x				Read nc	
	IOWrite					SWriteNA to IO space	x					
	afadd ‡‡					afadd (1 dw)	x				Read nc	
	afax					afax (2 dw)	x				Read nc	
	acswap					acswap (2 dw)	x				Read nc	
	aadd					aadd (1 dw)	x					
	aax					aax (2 dw)	x					
	Lsync_s_v					Lsync_s_v	x					
	Lsync_v_s					Lsync_v_s	x					Hold IRQ
	Msync					Msync	x					Bypass Mode On
	Msync P Msync V					Msync	x					
	Gsync					Gsync	x					

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†A "Read nc" ORB entry specifies that the returning data will not be cached. Both ReadNA amd ReadUC requests use "Read nc" ORB entries. (A ReadNA tells the Ecache not to allocate the line. A ReadUC tells the Ecache that the *P chip* will not be caching the line but the Ecache still should.)

‡Do more sophisticated match here (require pending or word match)

††Do more sophisticated match here (require pending or word match)

‡‡These five packet types are AMOs. The FOQ column indicates how many dwords of data accompany the request. Three of the AMOs return data, and two do not.

FIG. 4E